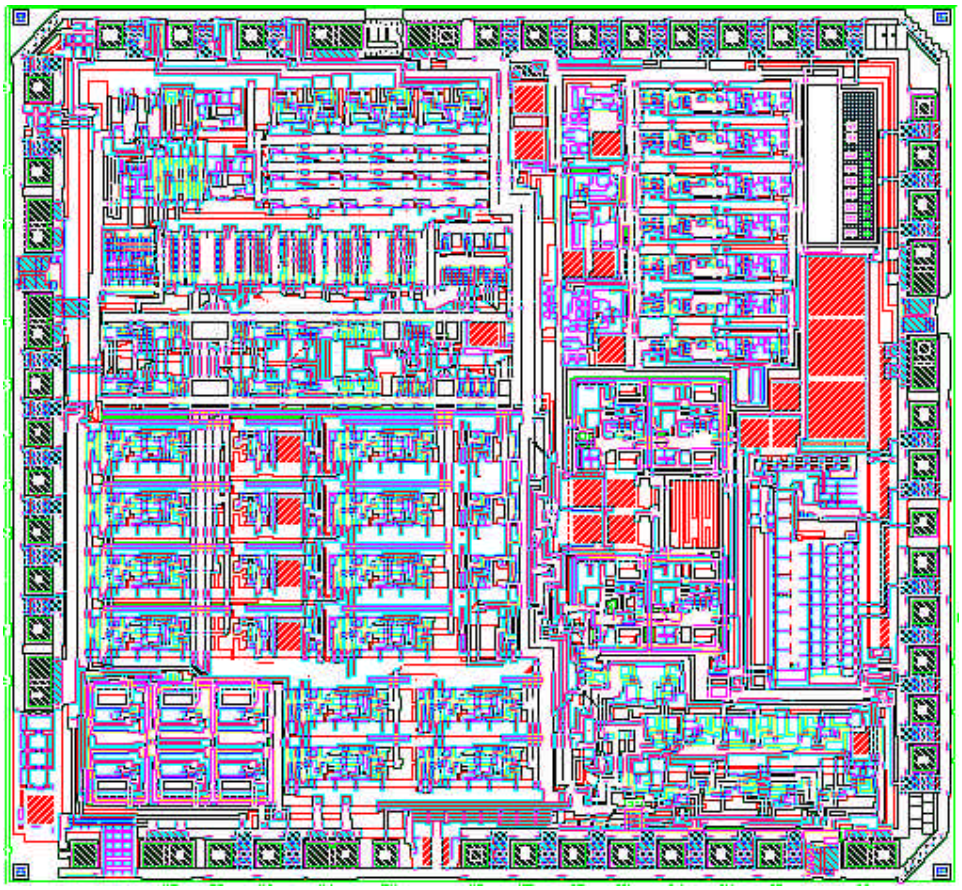
# FPPA2000 Specification and Description Document



# FPPA Specification Document

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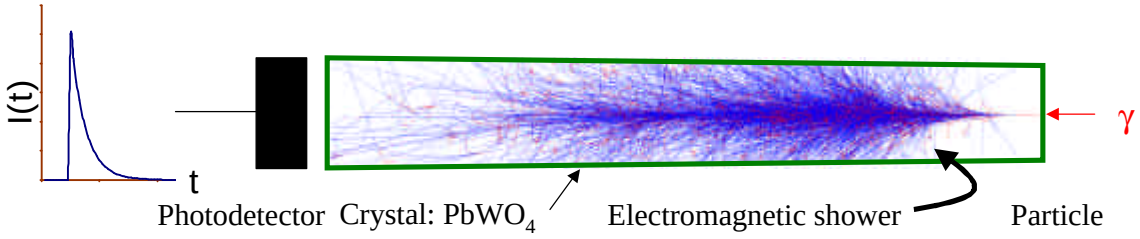
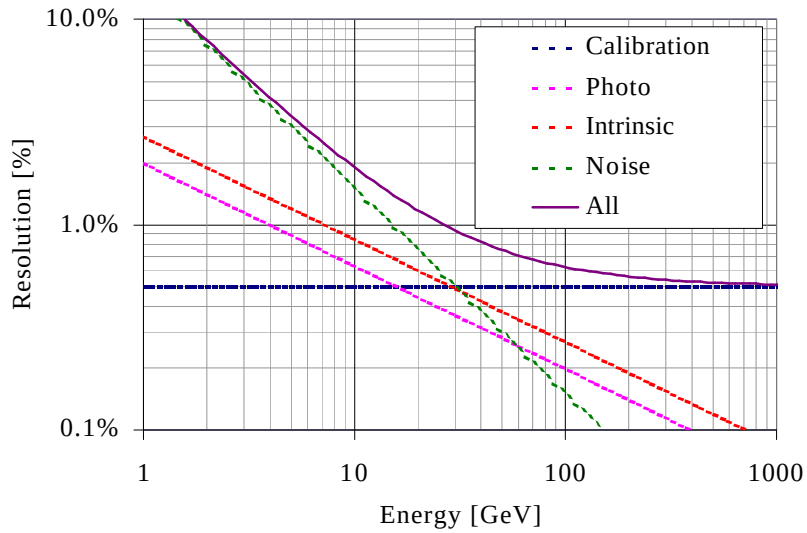
# 1. INTRODUCTION

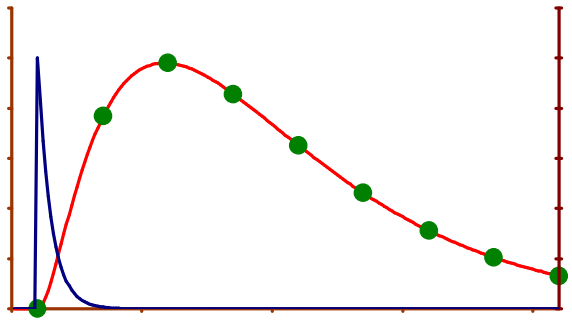
The CMS Electromagnetic Calorimeter (***ECAL***) will consist of ~80 000 scintillating crystals. Electromagnetically interacting particles create scintillation light in the crystals proportional to their energy. By measuring the amount of light, and knowing the crystal's location, the energy and position of the particle may be reconstructed. The interactions occur every ***bunch crossing***. The amount of energy deposited in a given crystal during a given bunch crossing is unrelated to the amount deposited during previous or subsequent bunch crossings.
A photodetector converts the scintillation light into a photocurrent. In the ***barrel*** part of the ECAL (the central cylinder of crystals), each crystal is equipped with two 25mm$^2$ silicon avalanche photodiodes (***APD***). The reverse-biased APD cathodes are connected together to sum the current. In the ***endcaps*** (the two disks of crystals at the ends of the cylindrical barrel), vacuum phototetrodes (***VPT***) are used.



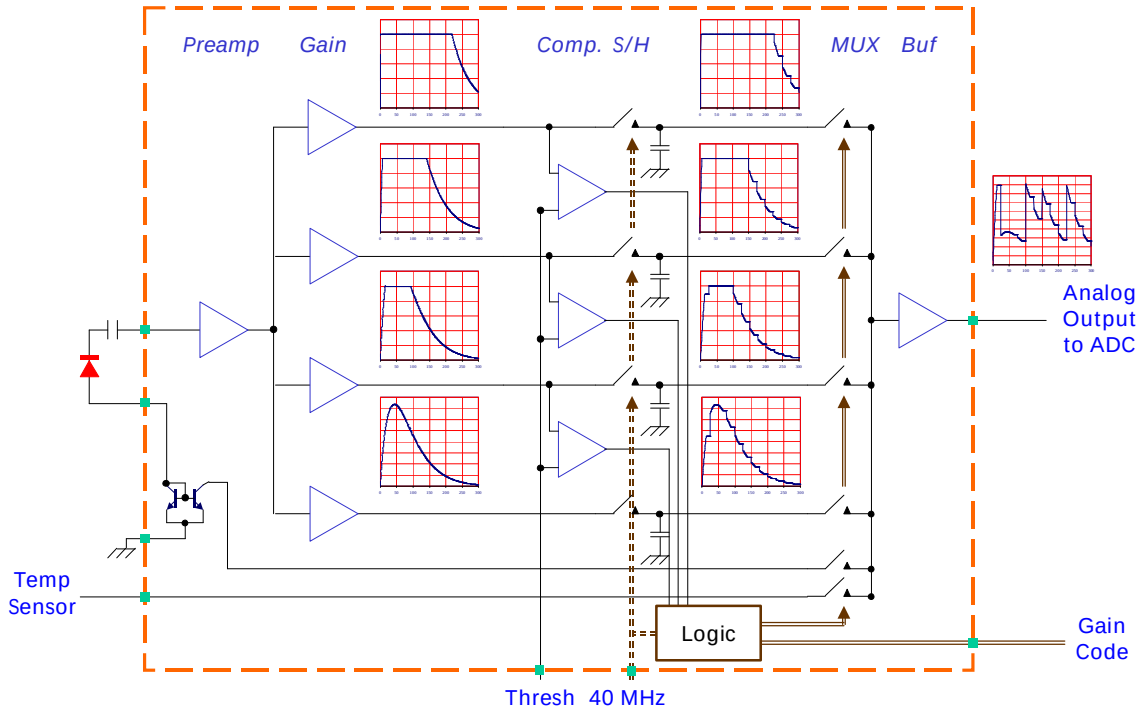

## 1.1. DESIGN CRITERIA




The ECAL requires a wide dynamic range, low noise readout in order to achieve its physics goals. The key design parameter is ***energy resolution***, which represents the precision with which particle energies are reconstructed. The energy resolution is the width of a histogram of reconstructed energy of particles of energy E from all locations in the calorimeter, divided by E. As shown in the graph, the resolution has several components. Intrinsic represents fluctuations in energy containment of the crystals. Photo represents the gaussian statistics in the number of photons produced (along with the excess noise factor of the photodetector). Noise is the contribution from electronic noise. Note that several crystals must be added together to reconstruct the energy, so that the individual channel noise is lower than that shown in the graph. In addition, as channels must be added, correlated noise must be kept to a minimum. Calibration represents our ability to maintain the energy calibration of all crystals across the detector. It also includes all residual electronic non-linearity or errors.



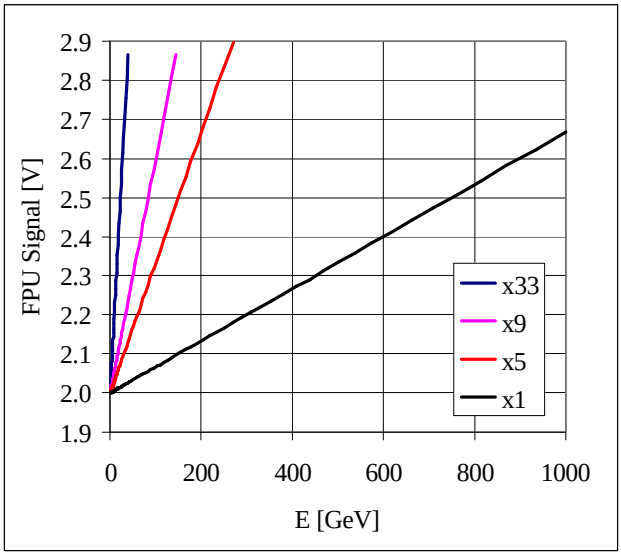
$PbWO_4$ is a relatively fast scintillator, with a principle decay time constant of 10 ns. We have chosen to make a voltage-sampling system running at the LHC collision frequency of 40 MHz. From a noise point of view, a long signal shaping time would be ideal. Due to the high background rate at the LHC, however, long shaping times add pileup noise. We have thus chosen 40 ns double integration (δ-function response $\frac{t}{t}e^{-t/t}$). The data collected for a given pulse are thus the dots shown above : the fast curve represents the scintillation light, the slower curve represents the shaped pulse being sampled, and the dots are the stored voltage samples. Via these samples, the amplitude - and hence energy - and timing of the incident pulse may be reconstructed.




In order to achieve the best performance, the signal acquisition and conversion electronics are mounted directly behind the crystals in the CMS detector. This sets constraints on the total power consumption, and on radiation hardness requirements, as the maximum dose in the barrel part of the detector is 1 MRad along with $2x10^{13}$ n/cm$^2$ (1 MeV equivalent) over the 10-year detector lifetime. Doses rise in the endcap region, and we will limit the placement of electronics such that the maximum lifetime radiation requirement is 2.5 MRad along with $5x10^{13}$ n/cm$^2$.

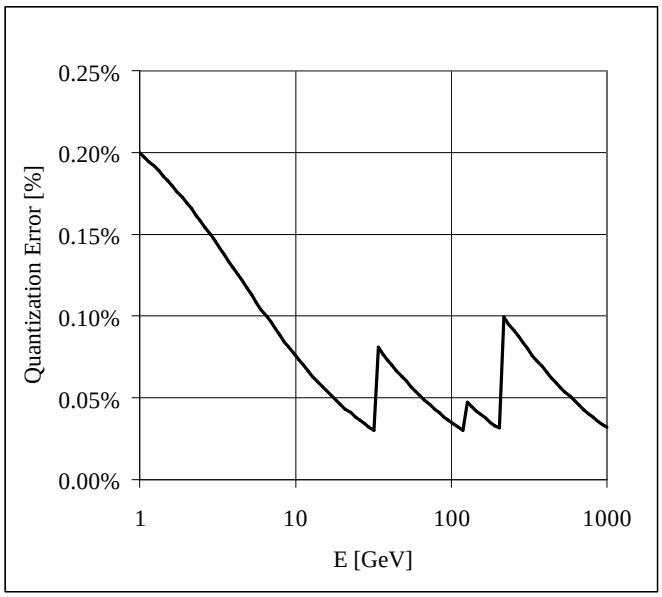
The figure above shows the basic acquisition scheme. The preamplifier is AC-coupled to the APD cathode (the APD is reverse-biased). Following the preamplifier are four gain stages, with gains 1, 5, 9 and 33. The gain stages have clamps to prevent saturation. The Floating Point Unit, which selects the gains and multiplexes them to an ADC, follows the gain stages. The FPU consists of a series of analog switches, comparators and digital logic. Directly after the gain, analog switches

are used to form a track/hold circuit. Comparators on the three highest gain stages along with digital logic determine which gain stage has the largest, non-saturated signal and multiplex that signal to the ADC via the output buffer. The digital logic also outputs a code indicating which gain range was used.




The gain stages consist of high open-loop gain non-inverting amplifiers, so that The gains have the form $1+R_2/R_1$. In order to have the same signal representation on all gain ranges, the bandwidth of the different amplifiers must be the same. In the original design concept, the bandwidths were fixed in the amplifier using $R_2$ and node capacitances, C. For optimal matching, the different $R_2$ and $C$ are formed by unit elements: $R_2 = nr$ and $C = mc$, hence we arrived at gains of 1, 5, 9 and 33. In FPPA2000, an improved scheme is used; in which the amplifiers themselves are high bandwidth, filtered by an RC filter afterwards. This eliminates the strict that the gains be precisely $1+2^n$, but we have kept 1, 5, 9 and 33 nonetheless.

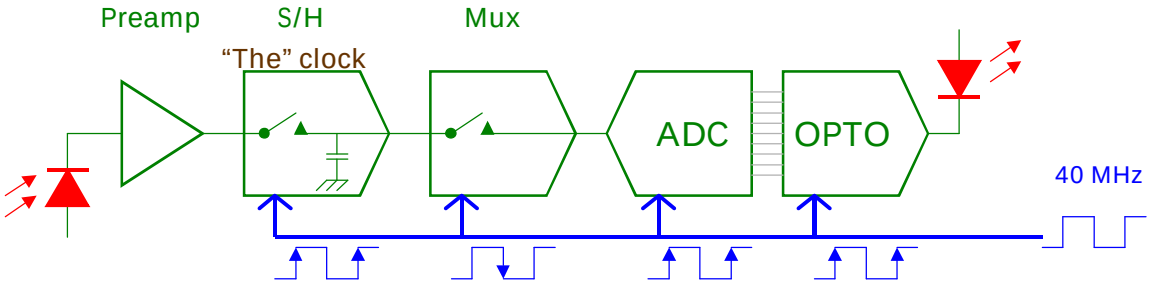
To relate the (peak) amplitude to energy (in the barrel) the FPU signal output (1.9 to 2.9V - to match the ADC input) - is shown above (assuming a 100 mV pedestal level). The comparator threshold is set at 80% of full-scale (i.e. for the plot shown on the left, the range changes once the signal reaches 800 mV).




A major design goal for the electronics is that it should not degrade the intrinsic energy resolution. With the multi-range scheme above, the contribution from the 12-bit ADC quantization error is given by the curve on the right. Here, the quantization error has been conservatively taken as $1/N$ rather than $1/\sqrt{12}N$, where N is the value of the ADC output code. The design target is to keep the error less than 0.1% for energies greater than around 20 GeV.

The complete readout channel consists of the FPPA followed by a commercial ADC (Analog Devices AD9042) and a custom optical link. One clock is used to control the three chips: The leading edge of the clock controls the S/H. The falling edge registers the comparators (thus

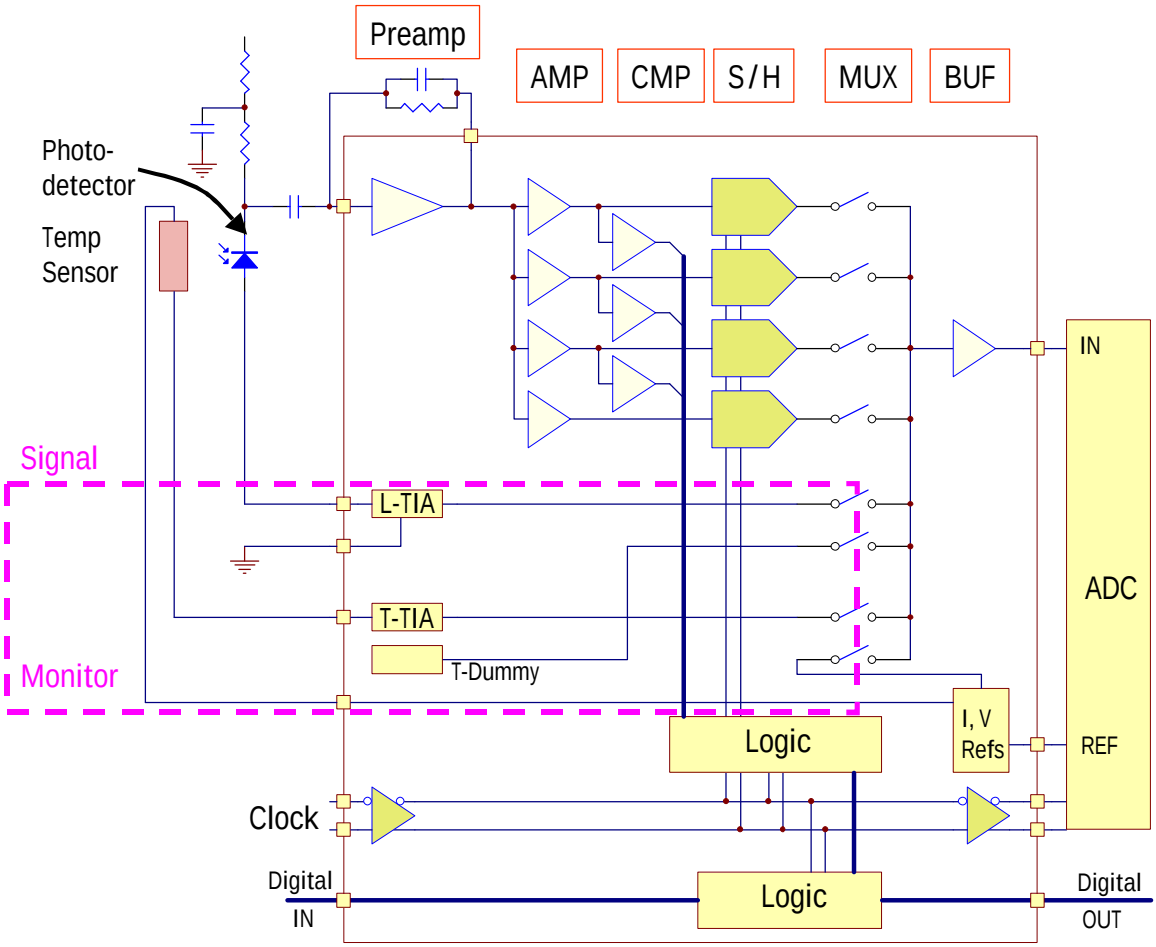
selecting the multiplexer setting) and the ADC encodes on the rising edge. The ADC includes an internal T/H, so that with the ADC acquisition time, as well as the transit time through the FPU, the ADC encodes the held level roughly 1ns before the T/H switches back to track mode. The FPU includes three clock period pipeline delays on the gain selection output bits in order to match the ADC latency.




Certain detector control functions are also included on-chip. As the APD leakage current increases with neutron fluence, it must be measured in order to correct the APD bias voltage (due to IR drops across the external APD series resistor). The APD leakage current is measured at the anode. In addition, both the crystal and APD are temperature sensitive, so circuitry to multiplex a temperature sensor to the ADC is also included. These functions are described in detail in Section 2.3.

## 2. BLOCK DIAGRAM

The FPPA consists of two primary functional blocks:
The ***Signal*** block contains all of the circuitry needed to acquire and condition the detector signal.
The ***Monitor*** block contains additional circuitry used to monitor the state of the detector (APD leakage current and APD+crystal temperature).




The block to the right ("ADC") represents the Analog Devices AD9042 12-bit ADC. This device was selected for use in the ECAL after extensive study. The FPPA design makes use of the temperature-compensated ADC reference to generate all bias voltages and currents, and the FPPA output stage has been specially designed for the AD9042 input stage. Both the FPPA and AD9042 are manufactured in bonded-wafer, dielectrically-isolated complementary bipolar technologies.

The various blocks inside of the FPPA are described below.

## 2.1. PREAMPLIFIER

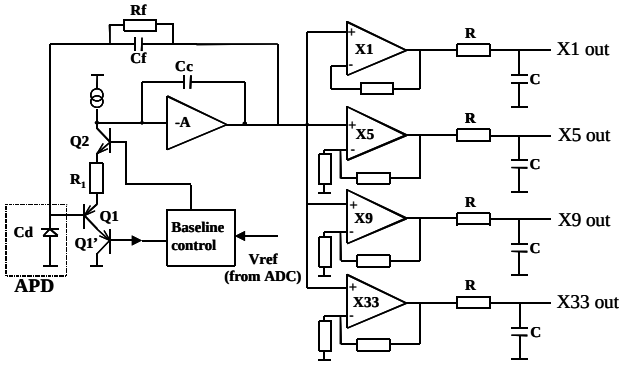
The preamplifier converts the sensor photocurrent into a voltage waveform to be sampled. Included in the preamplifier are the elements which shape the pulse. The overall gain of the pulse is fixed primarily by the external feedback resistor and capacitor. These components, along with internal resistors, capacitors and the input transistor, determine the pulse shape.
Four gain stages follow the preamplifier, **which is the only element in the FPPA covering the full dynamic range**. The ratios of internal metal resistors, which have low thermal coefficients and are radiation resistant, fix the values of these gains.

### *2.1.1. BARREL AND ENDCAP VERSIONS*

The detector capacitance figures in the expression for the noise and shaping time constants of the preamplifier. As the ***barrel*** and ***endcaps*** use different photodetectors, and have different full-scale charge, different versions are required. For simplicity, there is one layout, which can be changed from a barrel to an endcap version via a metal mask change. The only difference between a ***barrel*** FPPA and an ***endcap*** FPPA is in the preamp: the size of the input transistor, values of R and C filter components and the value of the external feedback resistor.

### *2.1.2. PREAMPLIFIER DESIGN*

The simplified schematic of the preamplifier and gain stages is shown below. The preamplifier converts the photocurrent into a voltage waveform to be sampled. The linear transimpedance amplifier topology was used instead of the charge amplifier due to its good capability to process signals for high dynamic range applications, and also for saving power dissipation because it does not require additional subsequent pulse shaping circuits. As seen from the schematic below, the passive $R_fC_f$ network associated with the compensation capacitance $C_c$, along with the detector capacitance $C_d$ and the resistance $R_1$ of the input stage performs the $(RC)^2$ shaping of the output pulse; therefore no additional shaping stage is needed. The shaping time constant has been fixed to $\tau$=40ns.




The full scale input charge of 60 pC, corresponding to a 1.5 TeV event in a crystal, gives an output pulse of 2V. The source capacitance is equal to 200 pF, cable capacitance included

An increase of the base current of $Q_1$, due to irradiation, also increases the voltage drop across $R_f$ and therefore decreases the output DC operating point of the preamplifier. A baseline control circuit has therefore been added to prevent DC voltage shift during operation. It consists of a

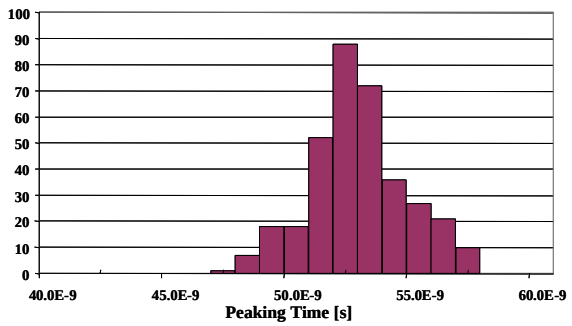
transresistance amplifier which tracks a copy of the input transistor base current trough $Q'_1$ and adjusts the base voltage of $Q_2$, keeping the output DC voltage constant.

The input PNP transistor was chosen to have a low intrinsic base resistor value (rbb') and the highest current gain β. The main sources of noise of the preamplifier come from the feedback resistor $R_f$, the base current of the input PNP transistor and the metal resistor $R_1$. The noise contribution of the collector current $I_c$ of $Q_1$ is negligible compared to the one of $R_1$. The equivalent noise charge referred to the input is given by:

$$ENC^2 = \left( \frac{2qIc}{b} + \frac{4kT}{R_f} \right) t + \frac{4kTR_1}{t} \left( C_d + C_f \right)^2$$

where τ is the shaping time constant, $C_f$ and $C_d$ are respectively the feedback and detector capacitance. The total simulated output noise (at the output of the x33 amplifier) is 55 μV rms corresponding to an ENC of 10000 electrons.

The preamplifier output pulse is sampled each 25 ns by subsequent S/H stages. In normal operation, the peak sample $P_k$ and its two neighbors will be summed to reconstruct the energy deposited in crystals. The $P_{k-1}$ sample, situated 25 ns before the peak, belongs to the rising part of the pulse, where its derivative dv/dt and therefore the current in the compensation capacitance $C_c$ are the highest. The exponential nature of the bipolar transistor causes pulse shape distortion (due to the nature of the feedback loop). A way of evaluating this change in shape versus the input charge is to study the variation of the ratio $r=P_{k-1}/P_k$. In principle, this ratio should remain constant over the whole dynamic range. Detailed calculations showed that 1% change of this ratio adds 0.5 ns to the reconstructed timing error and 0.2% to 0.5% (depending on the reconstruction algorithm) to the summed non linearity error, which remains more than acceptable in our case. The optimal solution for this problem is to insert a (metal) resistor between the emitter of $Q_1$ and $Q_2$. Simulation indicates that the variation of the $P_{k-1}/P_k$ ratio is around 1% when the transconductance $g_m$ of $Q_1$ and $Q_2$ is seven times more than $1/R_1$.



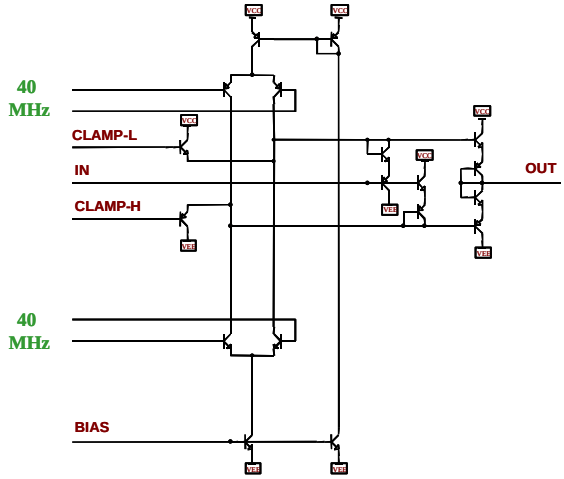

Monte Carlo simulations have been performed on the preamplifier. A set of 50 iterations, reflecting the lot to lot process variations along with on chip mismatches, was done on the peaking time spread. The figure on the left shows the results obtained. As a result, a 10 ns (peak-to-peak) peaking time spread is predicted between lots and chips will be sorted during production. In addition, the peaking time is correlated only to the absolute value of $R_1$.

The gain stages, connected directly to the output of the preamplifier, consist of closed loop current feedback amplifiers followed by simple RC filters, with a time constant much lower than the preamplifier shaping time constant. Each amplifier has a clamping circuit to prevent saturation and long recovering time for high level signals. The gains are fixed by the ratios of on-chip matched metal resistors which have low thermal coefficients and are radiation resistant.
In normal operation, analog sampled data provided to the ADC could belong to different ranges, depending on the input charge, coming from the photodetector. Therefore, the bandwidths of gain stages have to be close to each other in order to have a $P_{k-1}/P_k$ ratio variation on the order of 1%

when reconstructing the signal. The design strategy used to overcome this problem is to have a high closed loop bandwidth (250 MHz) for the amplifiers followed by matched RC filters which have a typical bandwidth of 30 MHz. Simulation indicates that the bandwidth mismatch between ranges has to be lower than 3% in order to have a $P_{k1}/P_k$ ratio variation lower than 1%. Matching data on passive components, provided by the foundry are much better than our needs.

## 2.2. FPU (FLOATING POINT UNIT)

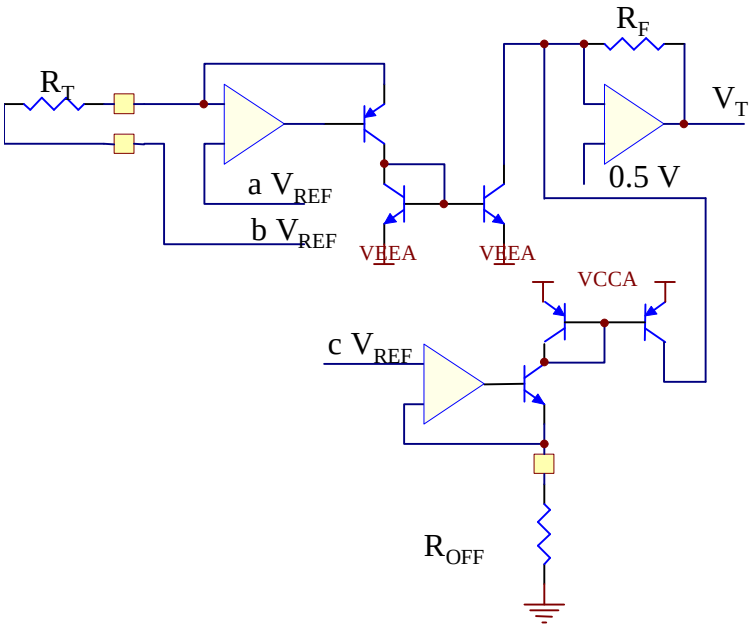
The FPU consists of analog switches, comparators and digital logic. Track/Hold circuits, which store the value of the sampled waveform, follow each gain stage. The 3 highest gain stages have comparators and digital logic, which selects the appropriate gain range - i.e. the highest gain below a fixed threshold. For normal data taking, the FPU operates in *auto* mode - i.e. it samples the waveform as described above. For test and calibration, *force* mode allows any of the FPU MUX switches to be selected.




The schematic of the switch used in track/hold and multiplexer stages is shown at left. In order to benefit from the high performance of the PN and PNP transistors a symmetrical switched emitter follower architecture was employed to realize both functions. Digitally controlled differential pairs turn on and off unity gain emitter followers, every 25 ns. A non-linearity of 2.6 $10^{-5}$ is achieved for signals up to 2.5V below the power rails. In addition, clamp transistors have been incorporated to improve speed.

## 2.3. TEMPERATURE AND LEAKAGE CURRENT (MONITOR)

### *2.3.1. TEMPERATURE MEASUREMENT*




A thermistor measures temperatures. Scaled copies of the ADC buffered reference are applied to the thermistor, as shown on the left. The "temperature voltage" is

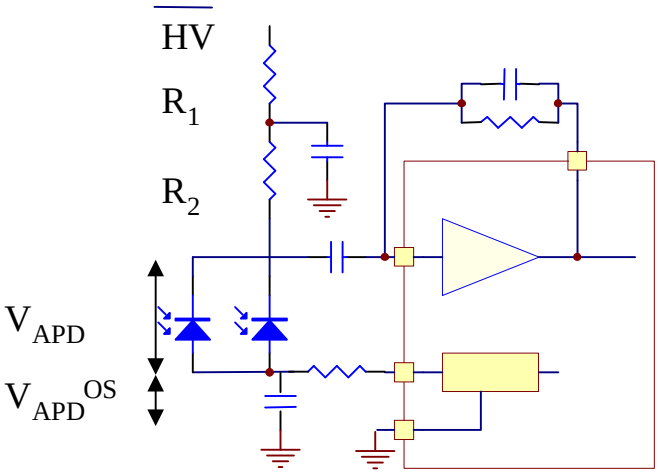
$$V_T = R_F\left[\frac{a}{R_T} - \frac{b}{R_T} + \frac{c}{R_{OFF}}\right]V_{REF} + 0.5$$

where $R_T$ is the resistance of the thermistor, of the form $R_T = Ae^{b/T}$. In order to minimize the full dynamic temperature range over the 12 bit of ADC, an offset (“0 °C”) voltage is subtracted.

As the ADC reference is used to set the current, the digitized value of $V_T$ does not change with radiation. In

order to monitor possible radiation effects (in the circuit), a dummy channel (the same circuitry, but connected to an internal, metal resistor) has been provided. As the dummy channel is identical to the temperature channel, it should track any changes.

### 2.3.2. LEAKAGE CURRENT MEASUREMENT




During operation, displacement damage due to radiation will cause an increase in the leakage current of the APDs. This current must be measured in order to (slowly) compensate the *IR* drop across the series resistors. As the APD gain is quite voltage sensitive ($\Delta Gain/Gain = 3.6\%/V$ at a gain of 50), the accuracy of measurement of ΔIR should be at the level of $\Delta V_{APD}$~20 mV to keep the gain error at the level of ~0.1%.
As shown on the left, the voltage across the APDs is

$V_{APD} = HV - V_{APD}^{OS} - (R_1 + R_2)(I_{LEAK1} + I_{LEAK2})$ where HV is the applied high voltage, $V_{APD}^{OS}$ is the input voltage of the leakage current measurement stage, and $I_{LEAK1}$ and $I_{LEAK2}$ are the leakage currents of the two APDs.

### 2.3.3. VREF MEASUREMENT

The last multiplexer switch sends a copy of $V_{REF}$ to the ADC. This allows a cross-check of any radiation damage or ageing in the $V_{REF}$ distribution circuit.

## 2.4. AUXILIARY FUNCTIONS

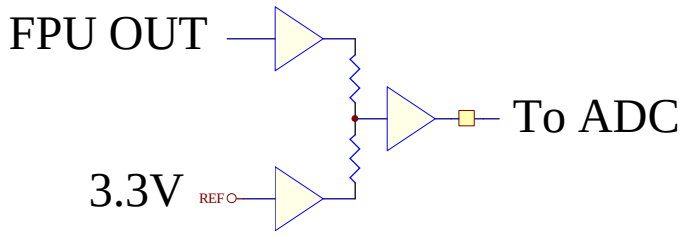
### 2.4.1. BIAS GENERATION

All internal bias currents and reference voltages are generated based on the 2.4V $V_{REF}$ output of the ADC. The ADC reference has a specified temperature variation of < 50 ppm/°C. Our measurements indicate a maximum gain change due to irradiation of <5 mV per LHC year, where an LHC year is defined to be 100 kRad ⊕ $10^{12}$ 1 MeV n/cm$^2$. This results in a "gain" change of 0.1% per LHC year (i.e. if 4096 ADC counts corresponded to 1.000 V at t=0, after 1 year, 4096 ADC counts correspond to 1.001 V).

### 2.4.2. CLOCK REGENERATOR

In order to reduce overall power consumption, the FPU regenerates the ADC clock. The clock regeneration circuit picks off the incoming PECL clock directly after it is buffered on chip. Levels are shifted to be compatible with the ADC clock input. This avoids 50Ω drivers and termination resistors for the ADC clock, as well as coupling capacitors to shift the level.

### 2.4.3. OUTPUT BUFFER




The output buffer drives the ADC. The ADC has a 1V signal swing (the input must be between the voltage reference 2.4V ±500 mV). In order to improve noise performance, though, the signal swing within the chip is 2V. The output buffer must therefore divide the signal by two, add the ADC offset of 1.9V, and provide sufficient drive to charge the parasitic capacitance as well as the 2 mA ADC static load. This is accomplished by 3 essentially identical amplifiers: one buffers a 3.3V reference created from the 2.4V reference; the second buffers the FPU OUTput (0.5V to 2.5V), and the third drives the ADC. The two resistors shown are equal, so the lowest voltage level output is (3.3V + 0.5V)/2 = 1.9V and the highest is (3.3V + 2.5V)/2=2.9V.

## 2.5. LOGIC

The static FPIN0…FPIN3 inputs program the operating mode of the FPU, as shown below. In ***Auto*** mode, the FPU runs automatically by selecting the appropriate signal range form the x1...x33 amplifiers. In ***Force*** modes, the multiplexer selects the given channel independent of the input at the preamplifier.

The multiplexer state of the FPU (i.e. which multiplexer was used on a given sample) is indicated by the FPO0 ... FPO2 outputs as shown below. In order to match the ADC latency, three clock cycles internally delay the outputs,.

The FPU does not latch the values of the control inputs FPIN0…FPIN3 as they are latched in the *CTRL* chip. The only stored digital information (which might be subject to corruption due to SEU) is in the *CTRL* chip, whose SEU performance has been shown to be suitable for the ECAL. These bits are read back separately (via the unused 16$^{th}$ *SERIALIZER* bits), so that the state of the system at any time is known.

### 2.5.1. PROGRAMMING THE FPU STATE

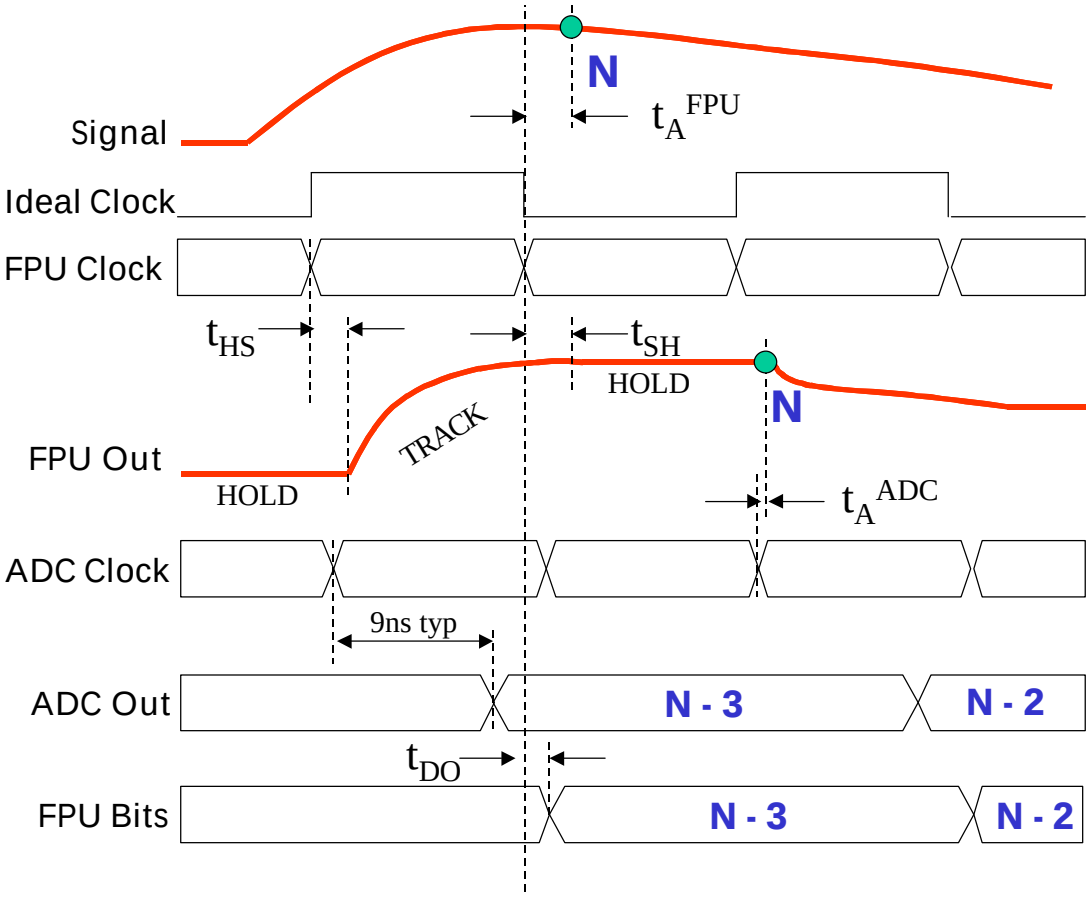
| ***Mode*** | ***FPIN3*** | ***FPIN2*** | ***FPIN1*** | ***FPIN0*** |
|---|---|---|---|---|
| Auto | 0 | X | X | X |
| Force x33 | 1 | 0 | 0 | 0 |
| Force x9 | 1 | 0 | 0 | 1 |
| Force x5 | 1 | 0 | 1 | 0 |
| Force x1 | 1 | 0 | 1 | 1 |
| Measure Temp | 1 | 1 | 0 | 0 |
| Measure Temp Dummy | 1 | 1 | 0 | 1 |
| Measure Leak | 1 | 1 | 1 | 0 |
| Measure $V_{REF}$ | 1 | 1 | 1 | 1 |

### 2.5.2. FPU DIGITAL OUTPUTS

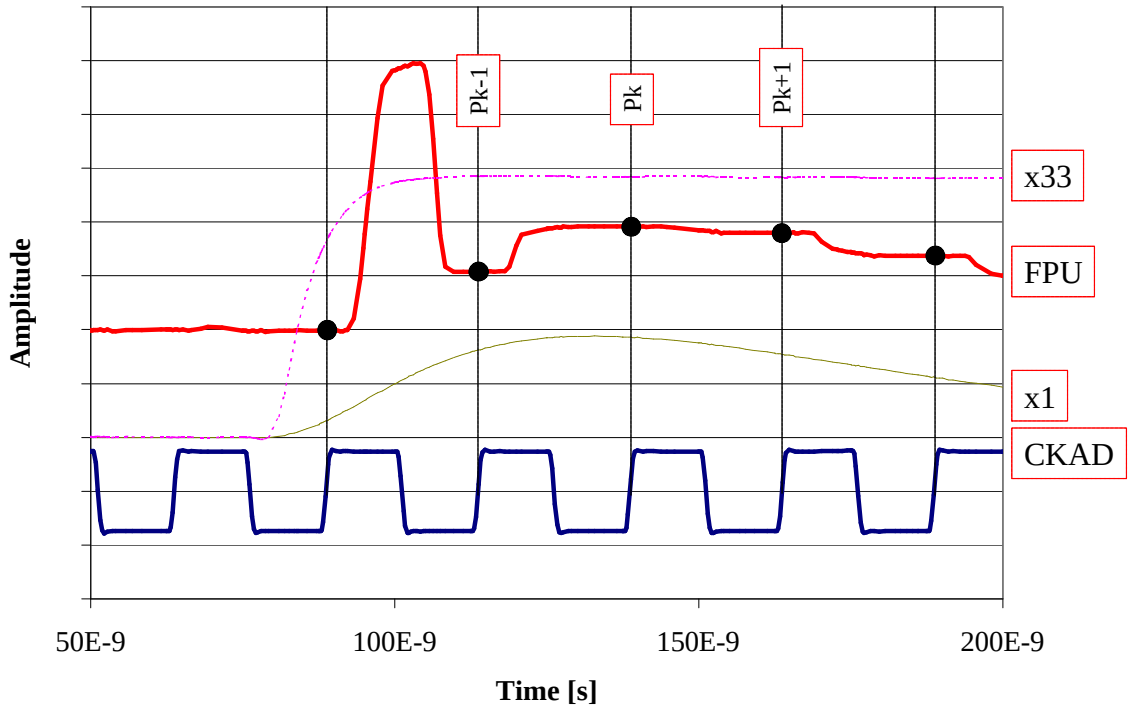
The outputs are delayed by three clock periods, as explained in Section 2.6.

| *Mode* | *FPO2* | *FPO1* | *FPO0* |
|---|---|---|---|
| Auto x33 | 0 | 0 | 0 |
| Auto x9 | 0 | 0 | 1 |
| Auto x5 | 0 | 1 | 0 |
| Auto x1 | 0 | 1 | 1 |
| Force x33 | 0 | 0 | 0 |
| Force x9 | 0 | 0 | 1 |
| Force x5 | 0 | 1 | 0 |
| Force x1 | 0 | 1 | 1 |
| Measure Temp | 1 | 0 | 0 |
| Measure Temp Dummy | 1 | 0 | 1 |
| Measure Leak | 1 | 1 | 0 |
| Measure $V_{REF}$ | 1 | 1 | 1 |

## 2.6. TIMING



The FPU timing is shown above. The FPU clock is a copy of the LHC 40 MHz clock, generated by the CTRL chip. As the clock is differential, the ideal clock in the figure above represents its "sign". When the *ideal clock* is high, the FPU tracks the signal, and when the *ideal clock* is low, the FPU holds all signals, and selects the multiplexer output. The ADC clock has the same phase as the FPU clock but the signal is sampled by the ADC just as the FPU returns to *hold* from *sample*. There is an 0.5 clock latency between the time when the signal is sampled by the FPU and when digitization commences. The ADC has a two clock plus 9 ns latency, to which the additional 0.5 clock latency of the FPU must be added. This results in an approximately 3 clock latency between when the signal was sampled, and the ADC data are valid. As the FPU output bits (FPO0 ... FPO2) must match the ADC, the FPU output bits are internally delayed by three clock cycles.

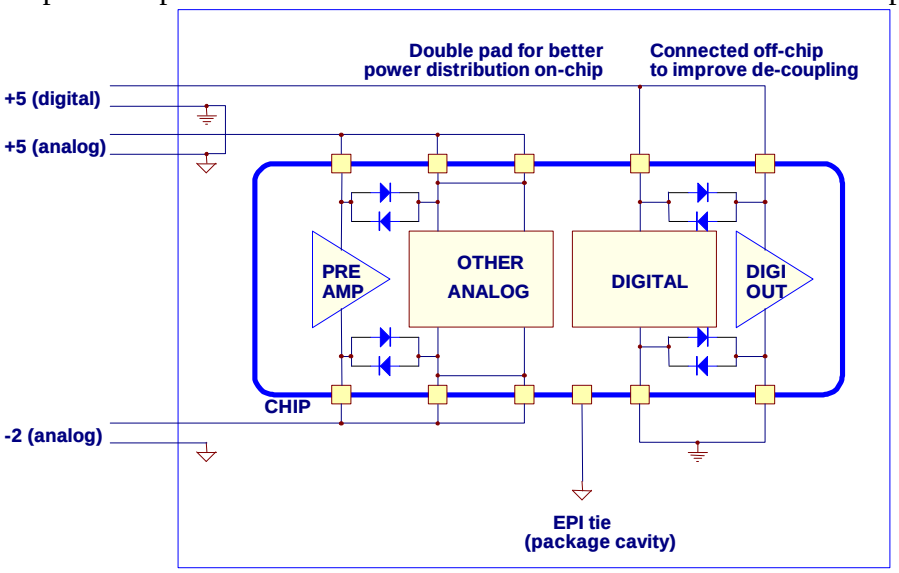



The operation is illustrated in the figure above: In this example, a very high-energy signal (~1 TeV) signal presents at around t=80 ns. **CKAD** is a single-ended representation of the clock as it appears at the ADC. **X1** and **x33** are the outputs of the x1 and x33 amplifiers, and FPU is the chip output to the ADC. The ADC encodes on the rising edge of **CKAD**, and the corresponding signal value is represented by a closed circle on the FPU waveform. Crudely, when **CKAD** is high, the internal T/H are in track mode. Thus, when the signal starts to develop, the T/H are holding. Slightly after t=100 ns, the T/H start to track, and – as there was no prior signal present – the x33 channel is active. The chip output (**FPU**) thus tracks the x33 which rises rapidly to the clamped value. Shortly after 100 ns, the internal logic selects the x1 channel (i.e. the rapidly rising edge near 100 ns represents the output tracking the x33 channel, and the rapidly falling edge is due to the internal switch from x33 to x1 channel). The next few samples continue on the x1 channel, and subsequently pass through the x5 and x9 channels (not shown).

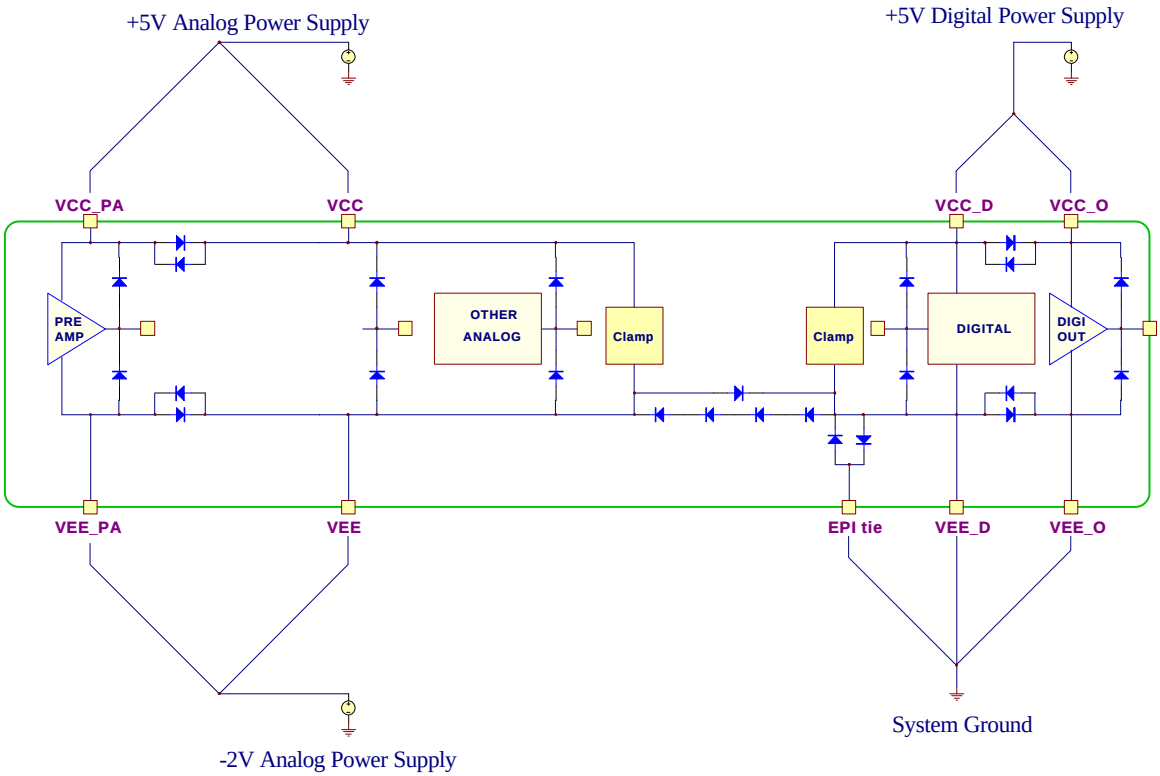
### 2.7. ESD PROTECTION

In order to prevent damage due to electro-static discharge, the core cell is surrounded by in most cases by diode-protected bond pads. The preamplifier and APD leakage current inputs are very sensitive to noise, hence a special ESD protection scheme was used for those pads. Differential

inputs are protected with two series diodes back-to-back. On-chip transient clamps protect the positive analog and digital supplies up to the design goal, which is the 1500V Human Body Model.




The basic power connection scheme is shown on the left. There are three supplies (+5 Digital, +5 Analog, -2 Analog) and one ground (Digital). In addition, there is a further connection (EPI tie) which connects to the "lost silicon" on top of the oxide layer which is not in the isolated trench of a component.




The ESD scheme is shown above. $V_{CCO}$ and $V_{EEO}$ are copies of $V_{CCD}$ (+5 Digital) and $V_{EED}$ (Digital Ground) used for digital output drivers, and are connected off-chip. Supplies are clamped as shown above. "Clamp" represents a transient clamp with 150 ns time constant. The digital and analog supplies are not clamped together (as they are separately powered, so their supplies may startup at different times)

# 3. FPPA SPECIFICATIONS

## 3.1. DESIGN CONSTRAINTS

"*Physics/Experimental Parameter*" are design inputs. The 2V preamp full scale output voltage was a design choice we made. The "*Derived*" requirements are then electrical requirements on the design based on the *Physics/Experimental* inputs.

### Barrel Readout FPPA

| ***Physics/Experimental Parameter*** | ***Symbol*** | ***Value*** | ***Unit*** |
|---|---|---|---|
| Full scale Energy[1] | $E_{MAX}$ | 1.5 | TeV |
| (Pb $WO_4$ Crystal Target) Light Yield | LY | 5 | p.e./MeV |
| APD Operating Gain | M | 50 | |
| Spread in Photoelectron Yield | ΔLY | ±10% RMS | p.e./MeV |
| Maximum Noise Level | $E_N$ | 40 | MeV |
| APD Capacitance[2] | $C_{APD}$ | <80 | pF |
| Interconnect Capacitance | $C_{KAPTON}$ | <30 | pF |
| Detector Capacitance (2 APD + Interconnect) | $C_{TOT}$ | <190 | PF |

| ***FPPA Electrical Requirement*** | ***Symbol*** | ***Value*** | ***Unit*** |
|---|---|---|---|
| (*Derived*) Full scale Charge | $Q_{MAX}$ | 60 | pC |
| (*Derived*) Noise Equivalent Charge | ENC | 10000 | $e^-$ |
| (*Derived*) Dynamic Range | DR | >90 | dB |
| Full scale Voltage (Preamp Output) | $V_{MAX}$ | 2 | V |
| (*Derived*) Noise Voltage | $V_N$ | 50 | μV |

[1]Readout in E not $E_T$ [2]Spread in $C_{APD}$ ~ 10%

### Endcap Readout FPPA

| ***Physics/Experimental Parameter*** | ***Symbol*** | ***Value*** | ***Unit*** |
|---|---|---|---|
| Full scale Energy[1] | $E_{MAX}$ | 3 | TeV |
| (Target) electron Yield[3] | LY | 34 | $e^-$/MeV |
| Spread in Photoelectron Yield[4] | ΔLY | ±20% RMS | p.e./MeV |
| Maximum Noise Level | $E_N$ | 100 | MeV |
| Detector Capacitance (VPT + Interconnect) | $C_{TOT}$ | <40 | pF |
| ***FPPA Electrical Requirement*** | ***Symbol*** | ***Value*** | ***Unit*** |
| (*Derived*) Full scale Charge | $Q_{MAX}$ | 16.5 | pC |
| (*Derived*) Noise Equivalent Charge | ENC | 3500 | $e^-$ |
| (*Derived*) Dynamic Range | DR | >90 | dB |
| Full scale Voltage (Preamp Output) | $V_{MAX}$ | 2 | V |
| (*Derived*) Noise Voltage | $V_N$ | 68 | μV |

[1]Readout in E not $E_T$ [3]Hamamatsu VPT, 5.5 pC/TeV [4]±10% LY, ±15% VPT

### 3.2. ELECTRICAL SPECIFICATIONS

## FPPA Power Supply

| *Parameter* | *Symbol* | *Value* | *Unit* |
|---|---|---|---|
| Positive Digital FPU Power | Vccd | +5 typ. | V |
| Positive Digital Output FPU Power | Vcco | +5 typ. | V |
| Positive Analog FPU Power | Vcca | +5 typ. | V |
| Positive Preamplifier Analog Power | Vccpa | +5 typ. | V |
| Negative Analog FPU Power | Veea | -2 typ. | V |
| Negative Preamplifier Power | Veepa | -2 typ. | V |
| Negative Digital FPU Power | Veed | 0 | V |
| Negative Digital Output FPU Power | Veeo | 0 | V |
| Power Dissipation | P | 750 | mW |

## Preamplifier

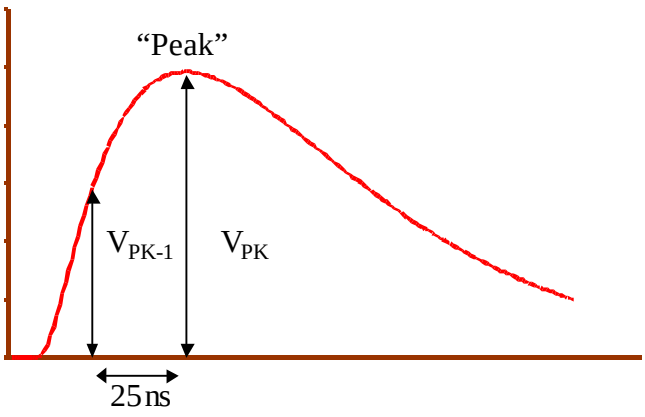
| *Parameter* | *Symbol* | *Value* | *Unit* |
|---|---|---|---|
| Gain Range "5"/Range "1" | $G_5$ | 5 | |
| Gain Range "9"/Range "1" | $G_9$ | 9 | |
| Gain Range "33"/Range "1" | $G_{33}$ | 33 | |
| Gain Tolerance | $\Delta G/G$ | ±1 | % |
| Preamplifier Pedestal Voltage[5] | $V_{PED}$ | 0.5 (min) | V |
| Pedestal Shift with irradiation | $d_{VPED}/dRad$ | 50 mV (max) | 10 years |
| Bandwidth Matching for Gain Stages | $\Delta BW/BW$ | 0.1 | % |
| Pulse shape Matching for Gain Stages[6] | $\Delta r/r$ | 1 | % |
| Clamp Voltage | $V_{CLAMP}^{PA}$ | 2.7 | V |
| Clamp Flatness[7] | $\Delta V_{CLAMPED}$ | 200 | mV |

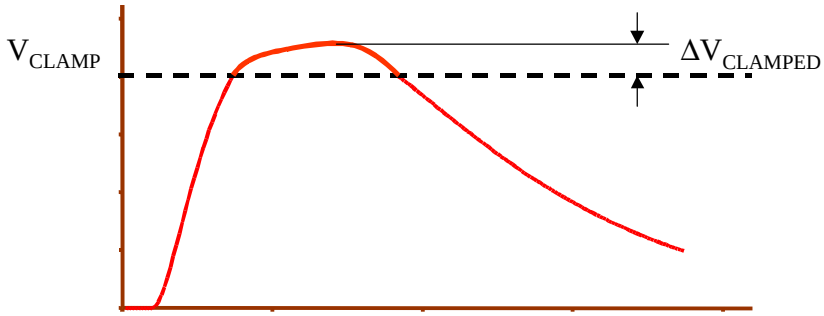
[5]Measured at the output of the preamplifier on the x33 range. The FPU output voltage is then $\left(V_{PED}+V_{3.3}+V_{OS}^{FPU}\right)/2$

[6]The variation of the value of r defines the pulse shape matching – r is the ratio of the preamp+gain stage output 25 ns before the peak sample value of the peaking time to that of the peak sample value of the peaking time -.

$$r=\frac{V_{Pk-1}(\text{Peaking time}-25\text{ns})}{V_{Pk}(\text{Peaking time})}.$$

The peak sample must satisfies $V_{PK} > V_{PK-1}$ and $V_{PK} > V_{PK+1}$.



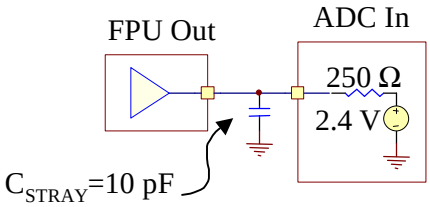



[7]Clamp flatness is the overshoot of the clamped output

## FPU

| *Parameter* | *Symbol* | *Value* | *Unit* |
|---|---|---|---|
| FPU Sampling Frequency | f | 40 | MHz |
| FPU Droop Rate | $V_{DROOP}$ | 0.2 | mV /ns |
| FPU Internal Linearity (deviation from best fit) | Lin(S/H) | 0.1 | % FS max |
| FPU Voltage Offset | $V_{OS}^{FPU}$ | 10 | mV |
| Comparator Overdrive to Switch | $V_{OD}$ | | mV |
| FPU Output Buffer Linearity[8] | Lin(BUF) | 0.1 | % FS max |
| FPU Output Buffer Noise | $V_N^{FPU}$ | 100 | µV |
| FPU Switching threshold (internally generated) | $V_{THRESH}$ | 2.1 | V |
| FPU Total Linearity (Signal) | Lin(FPU) | 0.1 | % FS max |
| FPU Output Range | $V_{OUT}^{BUF}$ | 1.9 to 2.9 | V |

[8]With the FPU Output terminated as shown




## Temperature / Leakage Current Measurements

| *Parameter* | *Symbol* | *Value* | *Unit* |
|---|---|---|---|
| T-Stage TransResistance | $R_F^T$ | 260[9] | kΩ |
| T-stage Offset (RTI) | $I_{OS}^T$ | 50 | nA max |
| T-Stage Linearity[9] | Lin(T) | 0.3 | % max |
| T-Stage Input Voltage | $V_{IN}^T$ | 1.2 | V |
| I-stage Current gain | G(I) | 10 | $\mu\Omega^{-1}$ |
| I-stage Offset (RTI) | $I_{OS}^I$ | 20 | nA max |
| I-Stage Linearity | Lin(I) | 1 | % max |
| I-Stage Input Voltage | $V_{IN}^I$ | 0 | V |
| I-Stage TransResistance | $R_F^I$ | 100 | kΩ |
| Input voltage current sensitivity | $dV_{IN}/dI_{IN}$ | 15 | Ω |

[9]Adapted to value of thermistor ($R_{25}$ = 100kΩ ; β = 3960 K)

# Auxiliary Functions

| ***Parameter*** | ***Symbol*** | ***Value*** | ***Unit*** |
|---|---|---|---|
| ADC Clock Output Central Voltage | $V_{CKA}$ | 1.6 | V |
| ADC Clock Output Swing (single output) | $\Delta V_{CKA}$ | ±400 | mV |
| ADC Clock Output Rise Time | $CKAt_R$ | TBD | ns |
| ADC Clock Output Fall Time | $CKAt_F$ | TBD | ns |

# Typical Operating Conditions (LHC)

| ***Parameter*** | ***Symbol*** | ***Value*** | ***Unit*** |
|---|---|---|---|
| Digital Logic +5V Supply | DVCC | +5.0 | V |
| Analog +5V Supply | AVCC | +5.0 | V |
| Analog –2 Supply | AVEE | -2.0 | V |
| Ambient Temperature (Environment) | $T_A$ | 18 | °C |
| Clock Frequency | LHC BCO | 40.08 | MHz |
| Minimum anticipated TD (η=0, 10 years) | $TD_{MIN}$ | 0.1 | MRad |
| Maximum anticipated TD (η=$\eta_{MAX}$, 10 years) | $TD_{MAX}$ | 2.5 | MRad |
| Minimum anticipated 1 MeV equivalent neutron fluence (η=0, 10 years) | $ND_{MIN}$ | $10^{13}$ | $n/cm^2$ |
| Maximum anticipated 1 MeV equivalent neutron fluence (η=$\eta_{MAX}$, 10 years) | $ND_{MAX}$ | $5x10^{13}$ | $n/cm^2$ |

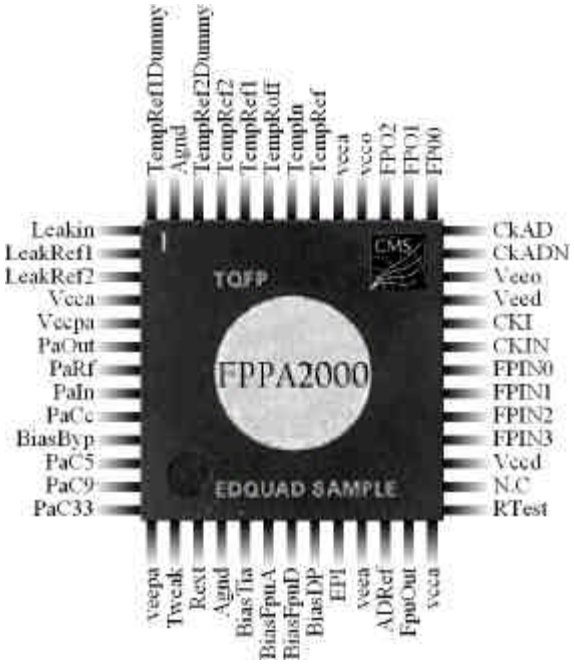
# 4. FPPA PINOUT, PACKAGE AND MECHANICAL INFORMATION

## 4.1. FPPA PIN FUNCTION DESCRIPTIONS

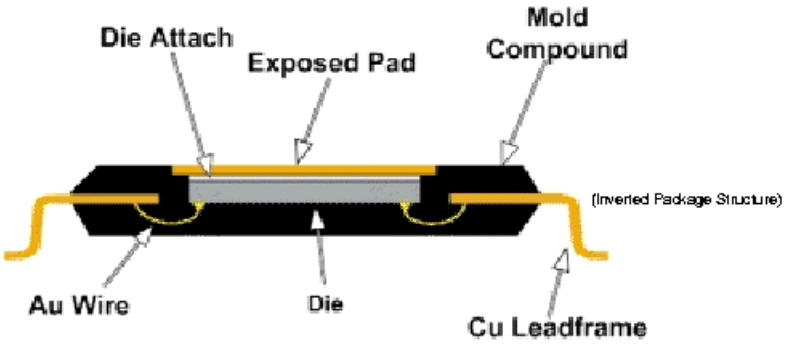
| Pin Name (Mnemonic) | Pin No. | Function |
|---|---|---|
| LEAK In | 1 | Connect to APD anode (not used for VPT) |
| LEAK $R_{F1}$ | 2 | Connect to LTIA feedback |
| LEAK $R_{F2}$ | 3 | Connect to LTIA feedback |
| PA Out | 6 | Connect to preamplifier feedback $R_F$, $C_F$ |
| PA RF | 7 | Used in fixing amplifier operating point |
| PA In | 8 | Input - connect to APD cathode/VPT anode through isolating capacitor |
| PA CC | 9 | Used in fixing amplifier operating point |
| BIAS BYP | 10 | Preamplifier bias generator decoupling capacitor |
| PA C5 | 11 | DC gain block for x5 decoupling capacitor |
| PA C9 | 12 | DC gain block for x9 decoupling capacitor |
| PA C33 | 13 | DC gain block for x33 decoupling capacitor |
| TWEAK | 15 | Used in fixing output buffer operating point |
| R EXT | 16 | Used in fixing bias generator operating point (I = 2.4V/R) |
| BIAS TIA | 18 | Bias generator decoupling capacitor |
| BIAS FPUA | 19 | Bias generator decoupling capacitor |
| BIAS FPUD | 20 | Bias generator decoupling capacitor |
| BIAS DP | 21 | Bias generator decoupling capacitor |
| AD REF | 24 | Connect to ADC $V_{REF}$ |
| FPU Out | 25 | Connect to ADC AIN |
| R TEST | 27 | Test Resistor. Not used |
| FP IN3 | 30 | FPU Control Bit 4 (TTL level) |
| FP IN2 | 31 | FPU Control Bit 3 (TTL level) |
| FP IN1 | 32 | FPU Control Bit 2 (TTL level) |
| FP IN0 | 33 | FPU Control Bit 1 (TTL level) |
| CK IN | 34 | Clock Input (Inverted) (PECL level) |
| CK I | 35 | Clock Input (Non-inverted) (PECL level) |
| CK ADN | 38 | Connect to ADC /ENCODE (Inverted) |
| CK AD | 39 | Connect to ADC ENCODE (Non-inverted) |
| FP O0 | 40 | FPU Digital Output Bit 1 (TTL level) |
| FP O1 | 41 | FPU Digital Output Bit 2 (TTL level) |
| FP O2 | 42 | FPU Digital Output Bit 3 (TTL level) |
| TEMP REF | 45 | Connect to thermistor |
| TEMP In | 46 | Connect to thermistor |
| TEMP ROFF | 47 | Used in fixing TTIA offset |
| TEMP $R_{F1}$ | 48 | Connect to TTIA feedback |
| TEMP $R_{F2}$ | 49 | Connect to TTIA feedback |
| TEMP $R_{F1}$ Dummy | 52 | Connect to Dummy TTIA feedback |
| TEMP $R_{F2}$ Dummy | 50 | Connect to Dummy TTIA feedback |
| EPI | 22 | Clean ground - die topside |
| VCC A | 4, 26 | +5V Analog Power Supply (Analog Part) |
| VCC PA | 5 | +5V Analog Power Supply (Preamplifier Part) |
| VCC D | 29 | +5V Digital Power Supply (Logic Part) |
| VCC O | 43 | +5V Digital Power Supply (Logic Output Part) |
| VEE D | 36 | 0V Digital Power Supply (Logic Part) |

| | | |
|---|---|---|
| AGND | 17, 51 | Analog Ground |
| VEE A | 23, 44 | -2V Analog Power Supply (Analog Part) |
| VEE PA | 14 | -2V Analog Power Supply (Preamplifier Part) |
| VEE O | 37 | 0V Digital Power Supply (Logic Output Part) |

## 4.2. FPPA PINOUT




## 4.3. FPPA PACKAGE

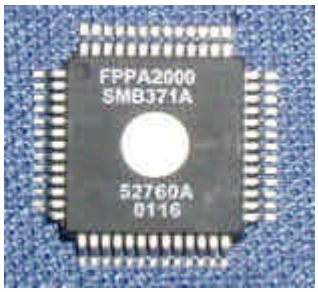



The FPPA will be packaged in a thermally-enhanced, 52-pin 10 x 10 $mm^2$ Thin Quad Flat Pack.

As shown on the left, the die is mounted upside-down, and is in contact with a metal plate. This allows a better thermal contact in the VFE readout modules. In order to simplify the module covers, the FPPA package has the same height as the ADC package.

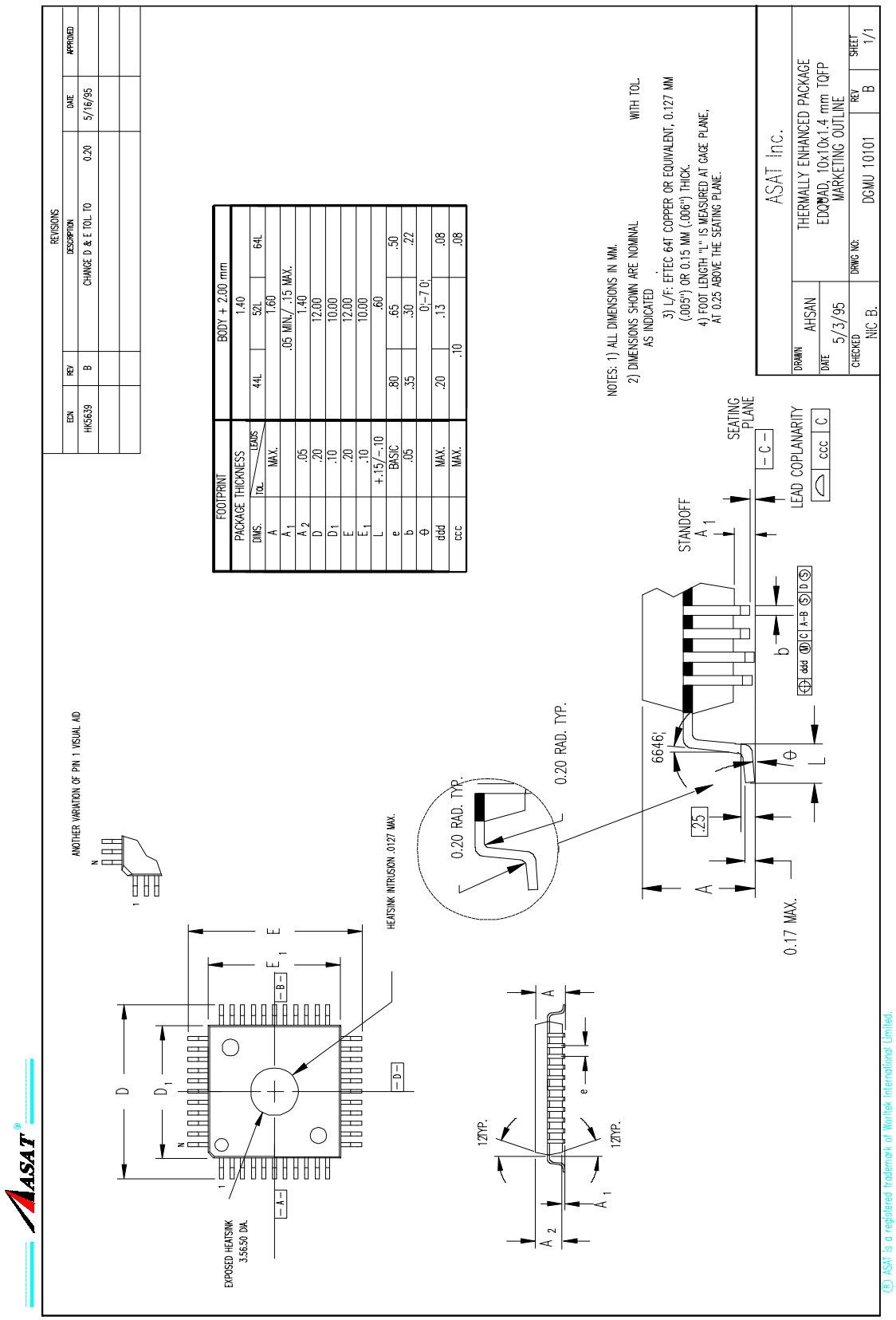
### 4.4. PACKAGE MECHANICAL INFORMATION

| | |
|---|---|
| Package Type | TQFP ASAT EDQUAD |
| Package Designation | JEDEC MS-026C BCC-H |
| Die size x | 5600 µ |
| Die size y | 5200 µ |
| Die thickness | Thinned for TQFP |
| Number of bonded pads | 52 |
| External lead pitch | 0,65 mm |
| Passivation | $Si_3N_4$ |
| Die attach | Conductive Epoxy |
| Bond wire | Gold |




The current FPPA package is shown at left. Final package marking will consist of

- Circuit name
- Mask set ID
- Date code


REVISIONS
ECN
REV
DESCRIPTION
DATE
APPROVED
HK5639
B
CHANGE D & E TOL. TO 0.20
5/16/95
FOOTPRINT
BODY + 2.00 mm
1.40
PACKAGE THICKNESS
LEADS
52L
64L
DIMS.
TOL.
MAX.
1.60
A
A1
.05 MIN./.15 MAX.
A2
1.40
D
12.00
D1
10.00
E
12.00
E1
10.00
L
+.15/-.10
.60
e
BASIC
.80
.65
.50
b
.05
.35
.30
.22
θ
0°-7°
ddd
MAX.
.20
.13
.08
ccc
MAX.
.10
.08
NOTES: 1) ALL DIMENSIONS IN MM.
2) DIMENSIONS SHOWN ARE NOMINAL WITH TOL. AS INDICATED.
3) L/F: EFTEC 64T COPPER OR EQUIVALENT, 0.127 MM (.005") OR 0.15 MM (.006") THICK.
4) FOOT LENGTH "L" IS MEASURED AT GAGE PLANE, AT 0.25 ABOVE THE SEATING PLANE.
ASAT Inc.
DRAWN AHSAN
DATE 5/3/95
CHECKED NIC B.
THERMALLY ENHANCED PACKAGE
EDQUAD, 10x10x1.4 mm TQFP
MARKETING OUTLINE
DRWG NO: DGMU 10101
REV B
SHEET 1/1
ANOTHER VARIATION OF PIN 1 VISUAL AID
EXPOSED HEATSINK 3.56x3.50 DIA.
HEATSINK INTRUSION .0127 MAX.
0.20 RAD. TYP.
0.20 RAD. TYP.
SEATING PLANE
STANDOFF
LEAD COPLANARITY
0.17 MAX.
12°TYP.
12°TYP.
ASAT is a registered trademark of Worltek International Limited.

## 5. REFERENCES


- AD9042 :12 bit, 41 MSPS monolithic A/D converter, Analog Devices Inc.
- J.P.Walder, J.M.Bussat, P.Denes, H.Mathez and P.Pangaud, “Custom Integrated Front-End Circuit for the CMS Electromagnetic Calorimeter”, *IEEE TNS*, 2001.
- P.Denes, J.M.Bussat, W.Lustermann, H.Mathez, P.Pangaud and J.P.Walder. “Light-to-Light Readout System of the CMS Electromagnetic Calorimeter”, *IEEE TNS*, vol 48, n° 3, pp. 499-503, 2001.